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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,931	07/19/2005	Helmut Theiler	14603-009US1/P2002,0626	2109

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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
11/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/521,931	THEILER, HELMUT	
	Examiner	Art Unit	
	ADI AMRANY	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 19-22* is/are pending in the application.

4a) Of the above claim(s) *12-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 22, 2008 have been fully considered but they are not persuasive. The amended limitation of "a logical detection signal" does not necessarily require that the signal is "digital." While logic gates may supply a digital output (0, 1), the claims have been amended with the adjective "logical" before detection signal.

The purpose of the Dalnodar diac (DC1) is to convert the analog output of the phase detectors (11,12) to a digital signal in order to control the triac (T1). One skilled in the art would readily be able to duplicate the Dalnodar diac such that one diac converts analog to digital and the second diac controls the triac. Converting analog to digital one step earlier in the Dalnodar process would be obvious and well within the level of ordinary skill in the art.

Regarding claim 6, the limitation of "logical load control signals" is distinguished from digital signals, as discussed above. If a user wishes to increase the speed of a fan by adjusting the manual controls, then the "logical" result would be to change the value of the variable resistor.

Lastly, applicant has not responded to the objection to claim 4.

Claim Objections

2. Claim 4 is objected to because there appears to be an unnecessary "is" at the end of line 1 ("logic unit is comprises"). Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Peil (US 4,560,909).

Peil discloses an electronic device (fig 1; col. 3-5) comprising:

an input (T1, T6) having leads to receive AC voltage;

a circuit array (11) for controlling a switch (18) to apply voltage to first (22) and second (23) loads based on whether a phase of the AC voltage is positive or negative and logical load control signals (20) generated separately for the first and second loads; and

a rectifier (D1-D6) that is connected to the input and that provides the voltage to the first and second loads, the voltage being generated from the AC voltage, wherein the rectifier comprises an open bridge circuit (D1, D3-D4, D6), and wherein the voltage comprises different half waves of the AC voltage, wherein a first half wave is applied to the first load and a second half is applied to the second load (col. 6, line 23 to col. 7, line 46).

Peil discloses that the circuit array (11) controls the triac switch (18) to apply voltage to the first load when the phase of AC voltage is positive only. This meets the limitation of a switch to "apply voltage to first and second loads based on whether a

phase of the AC voltage is positive or negative." In order to apply a voltage to the loads when the phase is positive and negative, the switch would always be on. This would render the switch useless. The rectifier provides the positive phase to the light (22) and the negative phase to the fan (23).

Peil also discloses that the logical result of manually changing the brightness of the bulb or the fan speed is the change in the load control signals (i.e. variable resistance 20).

With respect to claims 9 and 11, Peil discloses the variable resistor (20) generates a "load control signal" in response to a sensed condition, its resistance. And Peil discloses the circuit array "is part of" an integrated circuit (fig 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dalnodar.

With respect to claim 1, Dalnodar discloses a circuit array (fig 4-5; col. 4, line 47 to col. 6, line 37) for controlling operation of two loads (B5, B15) that operate with a rectified AC voltage (1, D5, D15), comprising:

a first current path that includes the first load (top half of 20, including lamp B15 and diode D15);

a second current path that includes the second load (bottom half of 20);

a semiconductor switch (T1) on a circuit path that includes the two loads, the switch being electrically connected to a common node (6) of the first and second current paths; and

a control unit (10, except for triac) to generate a switch control signal (output from diac DC1) that controls the semiconductor switch; wherein the control unit comprises:

a phase detection device (11, 12; col. 5, line 63 to col. 6, line 37) to detect whether a phase of the AC voltage is positive (D11) or negative (D12), and to output a detection signal that is based on whether the phase is positive or negative (Vc); and

a logic unit (diac DC1) to generate the switch control signal based on one or more load control signals (value of potentiometers, VR11-VR12) and the detection signal (Vc), wherein the control unit is configured to supply the first current path with a first half wave and to supply the second current path with a second half wave (figs 6a-b; col. 5, lines 34-46).

Dalnodar discloses that analog signals are passed from the phase detectors (11,12) to the diac (DC1). Dalnodar also discloses that the diac converts this signal to a digital signal in order to control the switching of the triac (T1). At the time of the invention by applicant, it would have been obvious to add additional diacs to the Dalnodar circuit in order to convert the signal to digital one step earlier, since it has been held that the mere duplication of the essential working parts of a device involves

only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (CCPA 1977).

As discussed above, "logical detection signal" does not necessarily require that the signal is "digital." Further, since the Dalnodar diac is a AD converter and logic unit to generate a switch control signal, it would be obvious to one skilled in the art to break the Dalnodar diac into two different components.

With respect to claim 2, Dalnodar discloses the control unit comprises a time control circuit (VR11-VR12) for generating the load control signals at a predetermined time (col. 5, line 63 to col. 6, line 37). Dalnodar discloses that the selected value of the potentiometers determines the switching time of the triac.

With respect to claim 3, Dalnodar discloses the control unit comprises a sensor circuit (VR11-VR12) for generating the load control signals in response to a sensed condition. Dalnodar discloses the control unit senses the values of the potentiometers and controls the switching time of the triac accordingly.

With respect to claim 4, Dalnodar discloses that the logic unit (diac D1) is only required to process one input at a time (fig 7; col. 6, line 44 to col. 8, line 2). The voltage across the capacitor (Vc) determines the timing of switching the triac (T1). The rate of charge of the capacitor is determined by the potentiometers (VR11-VR12). The interaction-reduction circuit (14) ensures that left over charge from one cycle (positive, for example) does not affect the other (negative cycle).

Dalnodar discloses that both half-cycle charge-rate control circuits (11, 12) share a capacitor (C1) and diac (DC1). At the time of the invention by applicant, it would have

been obvious to one skilled in the art to provide a respective capacitor and diac for each of the charge-rate control circuits (11, 12), since it has been held that the mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (CCPA 1977). With two inputs to the triac (T1), one skilled in the art would find it necessary to use a multiplexer in order to manage the timing of supplying two controls signals to one triac gate. The multiplexer would ensure that the control signal from the positive wave capacitor is applied only during positive half waves, as vise versa.

With respect to claim 5, Dalnodar discloses the circuit array "is part of" an integrated circuit (figs 4-6).

With respect to claim 6, Dalnodar discloses an electronic device (figs 4-6; col. 4-6), comprising:

an input having leads (4, 5) to receive AC voltage (1);

a circuit array for controlling a switch (T1) to apply voltage to first (B15) and second (B5) loads based on whether a phase of the AC voltage is positive (D11) or negative (D12) and load control signals (VR11-VR12) generated separately for the first and second loads; and

a rectifier (D5, D15) that provides the voltage to the first and second loads, the voltage being generated from the AC voltage (1), wherein the rectifier comprises an open bridge circuit, and wherein the voltage comprises different half waves of the AC voltage, wherein a first half wave is applied to the first load and a second half wave is applied to the second load (col. 3, lines 61-65).

As discussed above, it would have been obvious to duplicate the Dalnodar diac. *Id*. Dalnodar discloses that the rectifier is "downstream" of the loads. At the time of the invention by applicant, it would have been obvious to one skilled in the art to switch the bulbs (B5, B15) and diodes (D5, D15), since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA 1950). Switching the bulbs and diodes will not affect the performance of the Dalnodar device. The diodes will still direct one of two half waves to each load.

With respect to claim 7, Dalnodar discloses the phase detection device and logic unit, as discussed above in the rejection of claim 1.

With respect to claims 8-11, Dalnodar discloses the recited limitations, as discussed above in the rejections of claims 2-5, respectively.

With respect to claim 19, Dalnodar discloses that the switch comprises a single triac. At the time of the invention by applicant, it would have been obvious to one skilled in the art to substitute the Dalnodar triac with a MOSFET device, since the two components are art recognized switching devices. Both the triac and MOSFET connect input and output lead lines based on a signal received at their gate.

With respect to claim 20, Dalnodar discloses the circuit array is configured to apply a voltage to the first/second load when a phase of the AC voltage is positive/negative, as discussed above in the rejection of claim 1.

With respect to claim 21, Dalnodar discloses the switch is connected between ground (5) and the two loads (20).

With respect to claim 22, Dalnodar discloses the diac provides a logical 0 and a logical 1 to cause the triac to switch (col. 5, line 63 to col. 6, line 12). The diac would output a 0 and 1 regardless of where it is placed in the circuit (as the DAC connected to the output of the phase detectors, or as the switch control for the triac).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADI AMRANY whose telephone number is (571)272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

/Stephen W Jackson/
Primary Examiner, Art Unit 2836